NANO LETTERS

pubs.acs.org/NanoLett Letter

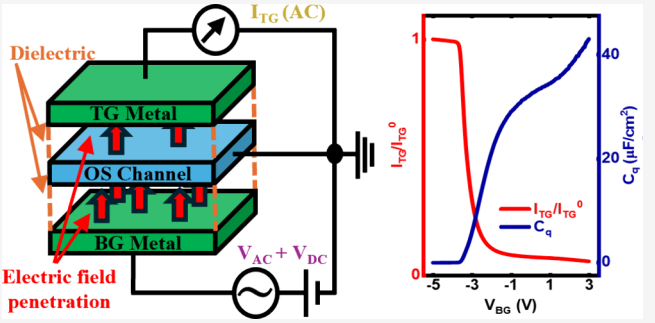
Direct Measurement of the Quantum Capacitance in Oxide Semiconductors Using an Electric-Field-Penetration Technique

Kisoo Nam,[†] Chang Niu,[†] Aravindh Shankar, Jian-Yu Lin, Sanjeev Khare, Sumi Lee, Pramey Upadhyaya, and Peide D. Ye*

Cite This: https://doi.org/10.1021/acs.nanolett.6c04248 Read Online

ACCESS | Metrics & More | Article Recommendations | Supporting Information

ABSTRACT: Indium-based oxide semiconductor (OS) field-effect transistors (FETs) have emerged as promising candidates for next-generation monolithic three-dimensional (3D) integration, but a limited understanding of channel capacitance hinders further scaling. Here, we measure quantum capacitance (C_q) in In-based OS channels by using a lock-in-based electric-field-penetration technique (eFPT). A small AC voltage modulation superimposed on the back-gate DC bias induces an electric field at the top gate, detected as an AC current (I_{TG}). Normalizing this current to its full depletion reference (I_{TG}^0) enables C_q extraction. Linear current scaling with frequency, excitation amplitude, and device area, together with an invariant normalized response, supports robust capacitance extraction. In the accumulation regime, an increase in C_q with DC bias is observed, which is consistent with band nonparabolicity and occupation of higher energy subbands. Finally, thicker InO_x channels and higher In concentrations in InGaZnO (IGZO) films exhibit a larger C_q. These findings demonstrate the feasibility of tailoring C_q in In-based OS FETs.



KEYWORDS: *electric-field-penetration technique, oxide semiconductor, indium oxide, indium−gallium−zinc oxide, quantum capacitance*

Device scaling remains a central objective in the semiconductor technology development.[1,2] To assess scaling progress, two key metrics—equivalent oxide thickness (EOT) and capacitance equivalent thickness (CET)—have been widely employed.[3−6] EOT has traditionally served as the primary figure of merit for Si metal-oxide-semiconductor field-effect transistors (FETs), where the channel density of states (DOS) is sufficiently high, and thus the channel capacitance does not significantly limit electrostatic gate control when EOT is larger than nanometer thickness.[7,8]

However, as devices continue to scale and emerging channel materials such as two-dimensional (2D) semiconductors and ultrathin oxide semiconductors (OSs) are introduced, this assumption breaks down. In these systems, the finite DOS gives rise to a non-negligible quantum capacitance (C_q), making CET a more appropriate metric for evaluating true electrostatic scaling.[9−11] For example, for $C_q = 20\ \mu F\ cm^{-2}$, the quantum capacitance contribution is approximately 0.17 nm. EOTs of 1 and 2 nm therefore correspond to CETs of approximately 1.17 and 2.17 nm, respectively ∼17% and 8.5% larger than the corresponding EOTs. As a result, understanding C_q has become increasingly important for next-generation device development.

Among emerging semiconductors, indium-based OSs have attracted significant interest as promising channel materials for FETs because of their compatibility with back-end-of-line processes for three-dimensional (3D) monolithic integration.[12−15] They also offer low off-state current,[16] high field-effect mobility,[17] large ON current,[18] and ultralow contact resistance.[19,20] Despite these advantages, their relatively high mobility and low DOS impose intrinsic limitations for device scaling because C_q can strongly influence the total gate capacitance and gate electrostatic control.[11,18]

To date, carrier-density-dependent C_q values in these systems have not been directly measured or systematically engineered. Instead, C_q is typically inferred from measurements of total capacitance (C_{tot}) and oxide capacitance (C_{ox}),[5,6] for example, using LCR-based techniques. However, such an indirect extraction becomes unreliable at low sheet carrier density (n_s), where the channel capacitance is small.[21,22] Even at high n_s, extrinsic parasitic capacitances and frequency-dependent dispersion can introduce substantial uncertainty.[23,24]

Here, we adapt the electric-field penetration approach established by Eisenstein et al.[25−29] to double-gate FETs

Received: August 27, 2026
Revised: October 27, 2026
Accepted: November 12, 2026

ACS Publications © XXXX The Authors. Published by American Chemical Society

Downloaded from pubs.acs.org/nalefd/article-pdf/doi/10.1021/acs.nanolett.6c04248/6921837/2/acs.nanolett.6c04248.pdf?guestAccessKey=e86e5cae-4f7e-4602-8685-84094555cb16 by PURDUE UNIV user on 18 November 2026

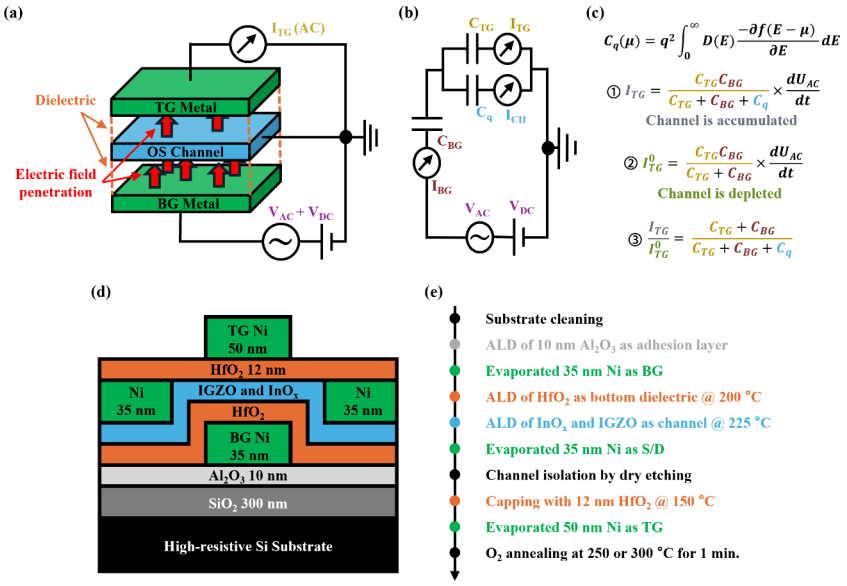


Figure 1. (a) Schematic illustration of the eFPT implemented in a double-gate OS transistor. A combined AC and DC bias is applied to the bottom gate, while the induced I_{TG} is monitored. (b) Equivalent circuit model of the eFPT measurement for the double-gate transistor. (c) Equations derived from the equivalent circuit. When the channel is accumulated, I_{TG} is limited by C_q, while in the depletion regime, I_{TG}^0 is determined solely by the oxide capacitance. The ratio I_{TG}/I_{TG}^0 therefore enables direct extraction of C_q. (d) Device schematic of the double-gate In-based OS FETs with varying In concentration of IGZO channels and different InO_x channel thicknesses. The bottom dielectric HfO_2 thickness is varied, while the top dielectric HfO_2 thickness is fixed. (e) Fabrication process flow for the double-gate transistors.

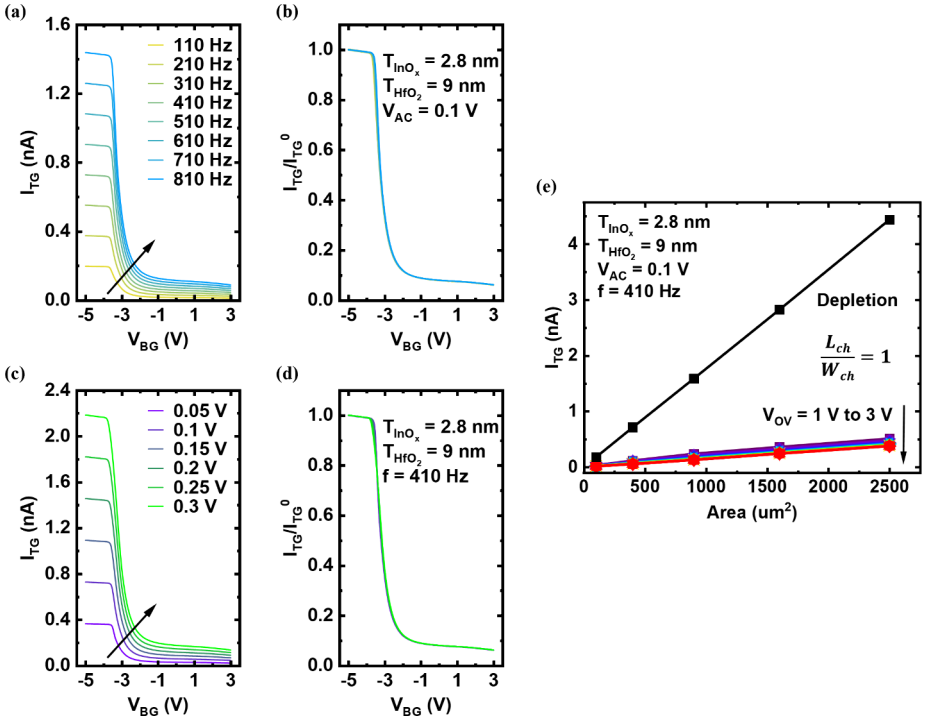


Figure 2. (a) Frequency dependence of I_{TG} measured on the same device at fixed V_{AC}. As the excitation frequency increases, the magnitude of I_{TG} increases proportionally. (b) Normalized ratio I_{TG}/I_{TG}^0 remaining unchanged over the entire frequency range. (c) AC voltage dependence of I_{TG} measured at fixed frequency. As the AC voltage increases, the magnitude of I_{TG} also increases proportionally. (d) Normalized ratio I_{TG}/I_{TG}^0 showing the same trend as the frequency-dependent result. (e) Measured area dependence on I_{TG}. For each device area, five devices were measured, and the averaged values are presented. Both the depletion and V_{OV} region exhibit a linear dependence on the device area, confirming the capacitive origin and quantitative reliability of the eFPT signal.

with ultrathin amorphous OS channels. This implementation enables quantitative extraction of carrier-density-dependent C_q in InO_x and InGaZnO (IGZO) transistor channels. As illustrated in Figure 1a, a combined DC bias (V_{DC}) and small AC excitation (V_{AC}) are applied to the back-gate to generate an electric field across the device channel. Due to the finite DOS in the ultrathin semiconducting channel, modulation of the chemical potential results in incomplete

https://doi.org/10.1021/acs.nanolett.6c04248
Nano Lett. XXXX, XXX, XXX−XXX

Downloaded from pubs.acs.org/naletd/article-pdf/doi/10.1021/acs.nanolett.6c04248/6921837/2/acs.nanolett.6c04248.pdf?guestAccessKey=e86e5cae-4f7e-4602-8685-84094555cb16 by PURDUE UNIV user on 18 November 2026

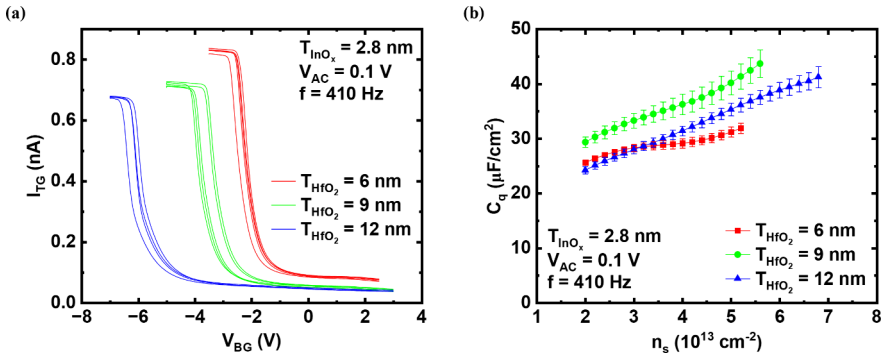


Figure 3. (a) Measured I_{TG} for devices with different bottom gate HfO_2 thicknesses (6, 9, and 12 nm), while maintaining the same InO_x channel thickness. A thinner bottom dielectric produces larger I_{TG} because of enhanced penetration of the AC electric field. (b) Extracted C_q as a function of n_s in the fully accumulated regime. Averaged values from five devices are shown for each dielectric thickness. Despite clear differences in raw I_{TG}, the extracted C_q exhibits consistent overall trends, confirming that eFPT reliably probes the intrinsic channel C_q independent of the bottom dielectric thickness.

electrostatic screening, allowing a penetration electric field to reach the top gate. This field is detected as an AC current at the top gate (I_{TG}) by using lock-in detection with high sensitivity and accuracy. The corresponding equivalent circuit and extraction formalism are shown in Figure 1b,c. In the full depletion regime, C_q does not contribute to I_{TG}, whereas in the accumulation and partial depletion regimes, I_{TG} becomes sensitive to C_q, enabling its direct extraction. Detailed double-gate device structure and fabrication flow are provided in Figure 1d,e.

We validate the robustness of this technique through the linear dependence of I_{TG} on the frequency, AC voltage, and device area along with a constant I_{TG}/I_{TG}^0 ratio. Although the bottom dielectric thickness changes the magnitude of I_{TG}, the extracted C_q exhibits consistent trends and comparable values across devices, confirming the validity of the analysis. In the accumulation regime, C_q increases with DC bias, consistent with theoretical calculations incorporating band nonparabolicity and the occupation of higher-energy subbands. Furthermore, temperature-dependent measurements (7−295 K) reveal a pronounced suppression of band-tail states at low temperature. Finally, we experimentally measured C_q of InO_x and IGZO with variations in thicknesses and compositions.

ROBUSTNESS OF THE ELECTRIC-FIELD-PENETRATION TECHNIQUE (EFPT)

To establish the validity of the eFPT, we systematically examined the dependence of I_{TG} on key experimental parameters. As described in Figure 1c, I_{TG} is proportional to the time derivative of the applied AC potential: $I_{TG} \propto dU_{AC}/dt = 2\pi f V_{AC}$, where f is the excitation frequency and V_{AC} is the AC amplitude. Because both the bottom dielectric capacitance (C_{BG}) and top dielectric capacitance (C_{TG}) scale with the device area, I_{TG} is expected to vary linearly with the frequency, AC amplitude, and device area, providing a direct experimental check of the measurement principle.

Figure 2a shows the frequency dependence of I_{TG} measured at a fixed V_{AC} = 0.1 V for a 2.8-nm-thick InO_x device with a 9 nm HfO_2 bottom dielectric. The measurements were performed on the same device (area = 400 μm^2) to eliminate device-to-device variation. In the depletion regime (V_{BG} = −5 V), where the channel carrier density is negligible, electrostatic screening is minimal, allowing the electric field to fully penetrate the channel, resulting in a large I_{TG}. As the back-gate voltage (V_{BG}) increases toward accumulation, mobile carriers progressively screen the electric field, thereby reducing the penetration and consequently decreasing I_{TG}. The magnitude of I_{TG} increases linearly with frequency, consistent with the expected proportionality to AC frequency f.

To further verify the robustness, Figure 2b presents the normalized current I_{TG}/I_{TG}^0, where I_{TG}^0 is the depletion regime current measured at V_{BG} = −5 V. The collapse of all curves onto a single curve across different frequencies confirms that the measurement is independent of the excitation frequency and reflects intrinsic device physics rather than measurement artifacts.

In Figure 2c, I_{TG} is measured at varying AC amplitudes (V_{AC} = 0.05−0.3 V) at a fixed frequency of 410 Hz. A linear increase in I_{TG} with V_{AC} is observed, as expected from the proportionality of the penetration field to the excitation amplitude. As shown in Figure 2d, the normalized I_{TG}/I_{TG}^0 again remains invariant, further confirming the validity and reliability of this technique. The extracted C_q values under different frequencies and V_{AC} conditions (Figure S2) show the same in excellent agreement.

Finally, the area dependence of I_{TG} is examined in Figure 2e. The averaged I_{TG} values from five devices with the same channel length (L_{ch}) and width (W_{ch}) are plotted as a function of the device area. In the depletion regime, I_{TG} exhibits a clear linear dependence on the area, as expected from capacitive scaling. To compare devices at an equivalent carrier density, I_{TG} is also evaluated at a fixed overdrive voltage ($V_{OV} = V_{BG} - V_{th}$), where the threshold voltage (V_{th}) is extracted from linear extrapolation of the drain current (I_D)−V_{BG} characteristics. A similar linear scaling is observed in this regime, confirming that the penetration current directly reflects channel capacitance.

Taken together, the linear dependence of I_{TG} on the frequency, AC amplitude, and device area, together with the invariance of the normalized I_{TG}/I_{TG}^0, demonstrates that eFPT provides a robust and quantitatively reliable platform for the direct extraction of quantum capacitance of the channel.

BOTTOM-DIELECTRIC-DEPENDENT QUANTUM CAPACITANCE

To investigate the influence of the bottom dielectric thickness on the extracted quantum capacitance, devices with three different HfO_2 bottom dielectric thicknesses were fabricated

https://doi.org/10.1021/acs.nanolett.6c04248
Nano Lett. XXXX, XXX, XXX−XXX

Downloaded from pubs.acs.org/naletd/article-pdf/doi/10.1021/acs.nanolett.6c04248/6921837/2/acs.nanolett.6c04248.pdf?guestAccessKey=e86e5cae-4f7e-4602-8685-84094555cb16 by PURDUE UNIV user on 18 November 2026

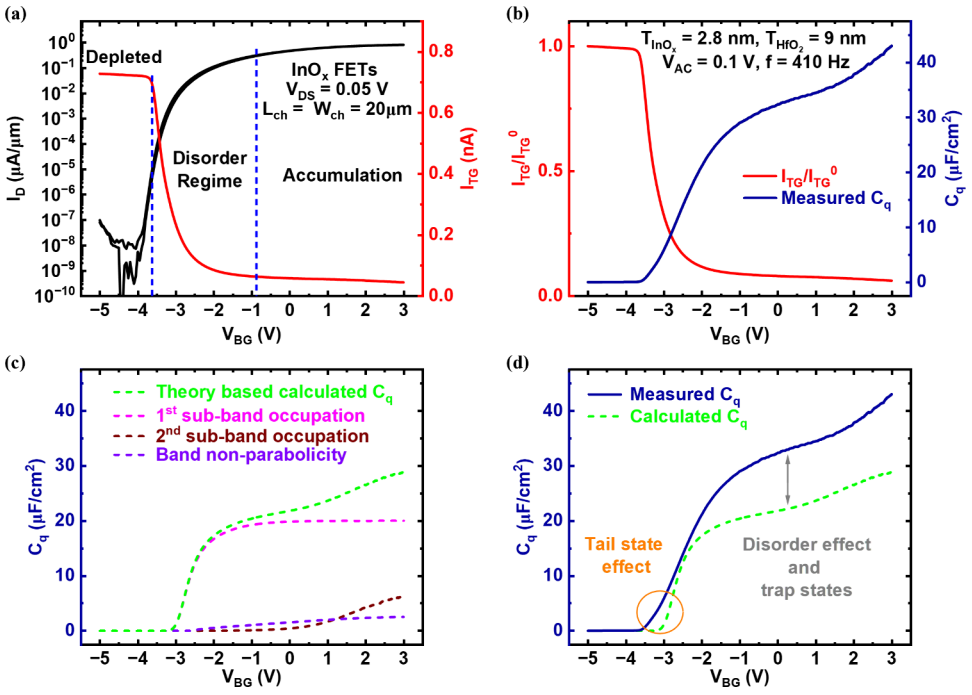


Figure 4. (a) Transfer characteristics of InO_x FETs with a 9-nm-thick HfO_2 bottom gate dielectric measured at V_{DS} = 0.05 with L_{ch} = W_{ch} = 20 μm. The corresponding I_{TG} is measured at the top gate with V_{AC} = 0.1 V and f = 410 Hz. (b) Normalized I_{TG}/I_{TG}^0 as a function of V_{BG}, where I_{TG}^0 is measured at V_{BG} = −5 V, and measured C_q based on the I_{TG}/I_{TG}^0 ratio. (c) Calculation from theory suggests that features in measured C_q are consistent with the sum of three contributions: population of the first subband (m^* = 0.3m_0), band nonparabolicity, and proximity to the second subband. (d) Comparison between the measured and calculated C_q. Enhanced measured C_q at low gate bias is attributed to band-tail states, whereas deviations at high gate bias are associated with disorder-induced states and trap-related contributions.

while maintaining the same InO_x channel thickness (2.8 nm). Figure 3a shows the measured I_{TG} for devices with bottom dielectric thicknesses of 6, 9, and 12 nm (L_{ch} = W_{ch} = 20 μm). As the bottom dielectric becomes thinner, the measured I_{TG} increases due to stronger penetration of the electric field through the thinner dielectric stack. Measurements from five devices under each condition show good reproducibility in the I_{TG} magnitude, with only minor variation in the threshold voltage.

Figure 3b presents the extracted C_q as a function of n_s. The corresponding bottom dielectric capacitances for the 6, 9, and 12 nm HfO_2 layers are C_{BG} = 2.10, 1.63, and 1.35 μF cm^{-2}, respectively. The top dielectric capacitance for the 12 nm HfO_2 layer is C_{TG} = 1.16 μF cm^{-2} (Figure S1). The carrier density is calculated using

$$qn_s = \int_{V_{ref}}^{V_{BG}} \frac{C_{BG}C_q(V)}{C_{BG} + C_{TG} + C_q(V)}\,dV \quad (1)$$

Here V_{ref} is the lowest measured bottom gate voltage in each data set, chosen within the depletion regime. The carrier density at this reference is assumed to be negligible, and $n_s(V_{ref})$ = 0 is therefore used. Integration proceeds from this reference to each V_{BG}. Experimentally extracted $C_q(V)$ is used throughout the integration, consistently incorporating its measured voltage dependence within the adopted equivalent-circuit model. Because C_q is determined as a function of the gate voltage before calculating n_s, no iterative process is required.

The plotted values in Figure 3b represent the mean extracted C_q from five devices for each dielectric thickness, with error bars indicating 1 standard deviation. These error bars characterize the observed device-to-device variation but do not independently quantify systematic uncertainties associated with I_{TG} and the oxide capacitance calibration.

Although the extracted C_q increases with the carrier density for all three bottom dielectric thicknesses, the values for the 9 nm devices are approximately 15−20% higher than those for the 6 and 12 nm devices at comparable carrier densities. No monotonic dependence on the bottom dielectric thickness is observed. Despite the same InO_x channel thickness, variations in the channel film properties and the dielectric channel interface may contribute to the observed differences. Nevertheless, the mean values obtained from five devices for each condition exhibit similar carrier density dependences and comparable C_q magnitudes across the three bottom dielectric thicknesses, supporting the reliability of eFPT for characterizing the quantum capacitance in OS channels.

EXTRACTION OF THE QUANTUM CAPACITANCE FROM MEASUREMENT AND CALCULATION

Figure 4a shows the transfer characteristics of a 2.8-nm-thick InO_x FET with a 9 nm HfO_2 bottom dielectric (L_{ch} = W_{ch} = 20 μm), together with the corresponding I_{TG} measured using eFPT (f = 410 Hz and V_{AC} = 0.1 V). The evolution of I_{TG} closely follows the electrostatic state of the channel across depletion, disorder-dominated, and accumulation regimes. In the depletion regime (large negative V_{BG}), the low carrier density results in negligible electrostatic screening, allowing the electric field to fully penetrate the channel and producing a maximum I_{TG}. As V_{BG} increases, carriers are gradually introduced to the channel, enhancing screening and reducing I_{TG}. In the intermediate regime, the device enters a disorder-dominated transport region, where conduction is governed by

https://doi.org/10.1021/acs.nanolett.6c04248
Nano Lett. XXXX, XXX, XXX−XXX

Downloaded from pubs.acs.org/naletd/article-pdf/doi/10.1021/acs.nanolett.6c04248/6921837/2/acs.nanolett.6c04248.pdf?guestAccessKey=e86e5cae-4f7e-4602-8685-84094555cb16 by PURDUE UNIV user on 18 November 2026

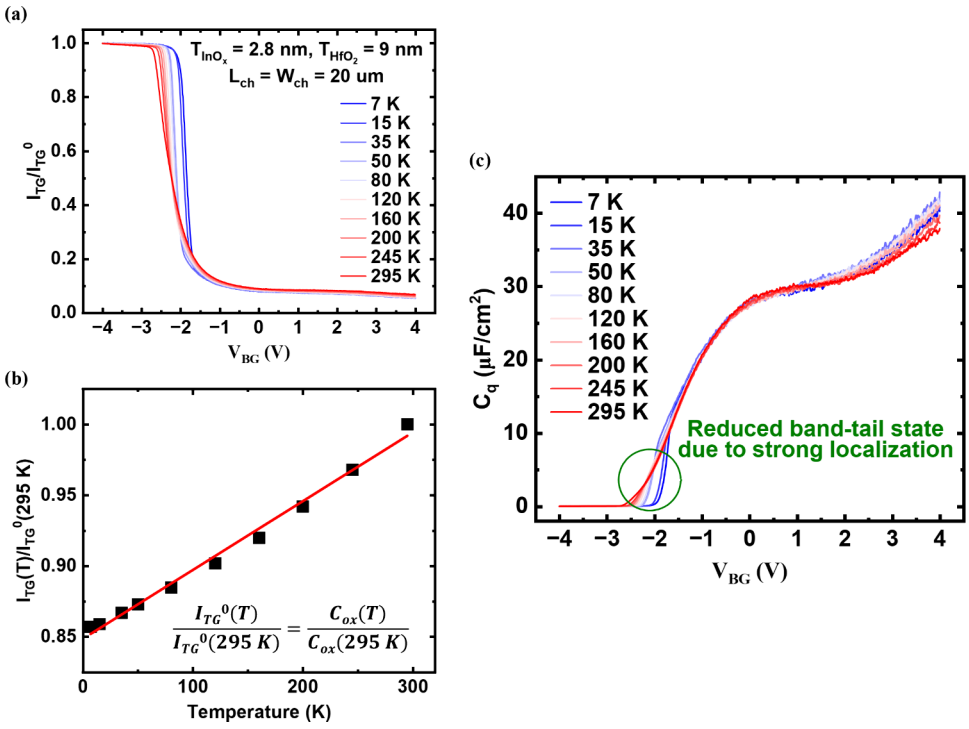


Figure 5. (a) Normalized I_{TG}/I_{TG}^0 ratio measured from 7 to 295 K for an InO_x (2.8 nm) device with a 9 nm HfO_2 bottom dielectric (L_{ch} = W_{ch} = 20 μm). As the temperature decreases, the transfer transition shifts positively and becomes sharper. (b) Temperature dependence of the depletion regime current ratio, $I_{TG}^0(T)/I_{TG}^0$(295 K), used to calibrate the temperature-dependent oxide capacitances, assuming both top and bottom dielectric C_{ox} decreases in the same ratio. (c) Extracted C_q as a function of V_{BG} at different temperatures after capacitance calibration. A pronounced reduction in C_q near threshold at low temperature is attributed to the suppression of band-tail states under strong localization, whereas C_q in the accumulation regime remains comparatively unchanged.

band-tail states associated with structural disorder in the OS.[30,31] The transport properties of an electron in atomically thin 2D amorphous OSs are complicated and need much more efforts to thoroughly investigate. In the accumulation regime, strong screening suppresses the penetration field, and the resulting I_{TG} directly reflects the quantum capacitance of the channel.

The normalized I_{TG}/I_{TG}^0 and extracted C_q as a function of V_{BG} are shown in Figure 4b. The extraction is performed using C_{BG} = 1.63 μF cm^{-2} and C_{TG} = 1.16 μF cm^{-2} (Figure S1). In the depletion regime, C_q is negligible due to the absence of mobile carriers. As V_{BG} increases beyond ∼−3.5 V, C_q rises rapidly, corresponding to the onset of carrier accumulation. At higher gate bias, C_q continues to increase, indicating a progressive enhancement of the DOS with increasing chemical potential.

Finite channel charging times must be considered when interpreting AC-based eFPT measurements, particularly in the high-resistance regime near the threshold. To assess the validity of the quasi-static approximation under our measurement conditions, we analyzed the device response using a one-dimensional distributed RC model. Details of the analysis are provided in Figure S3.

The capacitance extracted by eFPT reflects the small-signal electronic screening response, including contributions from interface and border traps that exchange charge with the channel at the measurement frequency. It should therefore be interpreted as an effective channel capacitance that includes the channel DOS contribution and any responding trap contributions. Interface trap capacitance (C_{it}) has a greater relative influence near the threshold, where the channel capacitance is small. In accumulation, the larger channel capacitance is expected to reduce its relative influence. An approximate analysis of the subthreshold swing yields an interface trap capacitance of C_{it} = 1.27 μF cm^{-2}, corresponding to approximately 3% of the capacitance extracted in a fully accumulated regime. Assuming that C_{it} remains of comparable magnitude in this regime, its contribution is small relative to the channel DOS contribution. Band-tail and defect states within the amorphous channel may also contribute to measurement. These states belong to the DOS of the actual disordered channel and are distinct from the ideal band DOS.

Depletion-related contributions were considered within the same modeling framework. Our quantitative interpretation focuses on the accumulated regime, where the semiconductor charge response is represented by the channel quantum capacitance and any responding trap contributions; a separate bulk depletion width response is not included. Under negative gate bias conditions, the ultrathin channel is assumed to remain fully depleted throughout the small AC perturbation. Assuming a fixed ionized donor charge, the depletion region spans the entire film thickness, and the associated depletion charge does not vary appreciably with the AC perturbation. The differential capacitance associated with the depletion-width modulation is therefore neglected. Furthermore, we treat the ultrathin channel as a single electrostatic node, neglecting potential variations across its thickness.

To elucidate the origin of this increase in extracted C_q, we perform theory-based calculations of C_q, as shown in Figure 4c. The model considers three key contributions: (i) occupation of the first subband, (ii) occupation of the higher-energy (second) subbands, and (iii) band nonparabolicity. Assuming

https://doi.org/10.1021/acs.nanolett.6c04248
Nano Lett. XXXX, XXX, XXX−XXX

Downloaded from pubs.acs.org/naletd/article-pdf/doi/10.1021/acs.nanolett.6c04248/6921837/2/acs.nanolett.6c04248.pdf?guestAccessKey=e86e5cae-4f7e-4602-8685-84094555cb16 by PURDUE UNIV user on 18 November 2026

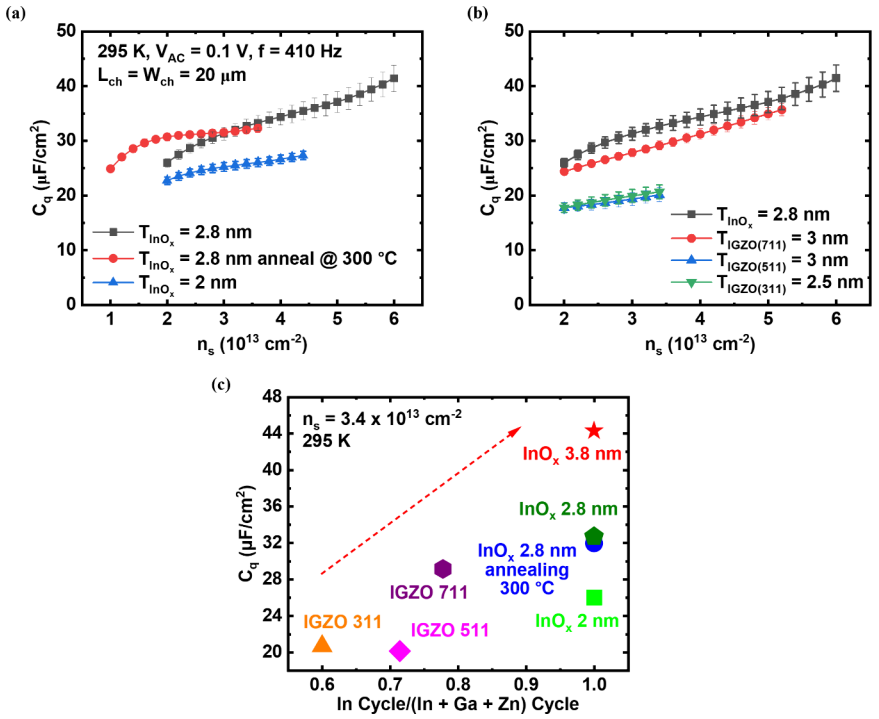


Figure 6. (a) Extracted C_q as a function of n_s for InO_x FETs with different channel thicknesses. Thicker InO_x channels exhibit higher C_q, reflecting an increased accessible DOS at thicker film. (b) Extracted C_q for OS FETs with different In concentrations at comparable channel thicknesses. Devices with lower In concentration show smaller C_q. (c) Summary of extracted C_q at a fixed $n_s = 3.4 \times 10^{13}$ cm^{-2} as a function of the In cycle ratio for In-based OSs. The C_q data for the 3.8 nm InO_x channels were obtained from large devices.

an effective mass of $m^* = 0.3m_0$, the first subband contribution exhibits a rapid increase in C_q to approximately 20 μF cm^{-2}, consistent with an ideal 2D DOS model. However, the InO_x channel is not strictly 2D, and its conduction band deviates from a simple parabolic dispersion. Accordingly, band nonparabolicity is incorporated to account for the gradual increase in the DOS with energy. In addition, occupation of higher subbands becomes increasingly important at large V_{BG}, further enhancing C_q. The calculated C_q depends on the assumed effective mass through the subband DOS amplitude, D_0. At all other fixed model parameters, the corresponding subband contributions to C_q scale linearly with m^*.

Figure 4d compares of the measured and calculated C_q. The combined contributions from the subband occupation and band nonparabolicity reproduce the overall trend of the experimental data, although quantitative discrepancies remain. We ascribe this discrepancy to the unavoidable bulk defects and interface traps. At low carrier density (negative V_{BG}), the measured C_q exceeds the calculated values due to contributions from band-tail states,[30,31] which introduce additional DOSs not captured in the ideal model. At high gate bias, disorder-related modifications of the channel DOSs and contributions from trap states are possible contributors for further enhancement of the measured C_q.

Importantly, extracted C_q has direct implications for electrostatic scaling. In the low-carrier-density regime, C_q becomes comparable to C_{ox}, indicating that the channel capacitance significantly limits the total gate capacitance. Even at high carrier density, C_q remains finite and non-negligible, deviating from the sufficiently high DOS assumption commonly used in the conventional scaling analysis. As a result, the CET, which incorporates both C_{ox} and C_q, provides a more realistic metric for an effective electrostatic thickness than the EOT alone. These results demonstrate that C_q must be explicitly considered in OS channel devices, particularly under low-density and near-threshold operation regimes, where it fundamentally limits the scaling performance.

Overall, these findings highlight that eFPT enables the direct and quantitative evaluation of C_q across the full operating regime, providing critical insight into CET-limited scaling in emerging OS systems.

TEMPERATURE-DEPENDENT QUANTUM CAPACITANCE MEASUREMENT

To investigate the temperature dependence of C_q, eFPT measurements were performed on the same 2.8-nm-thick InO_x device with a 9 nm HfO_2 bottom dielectric over a temperature range of 7−295 K (f = 210 Hz and V_{AC} = 0.1 V). The normalized I_{TG}/I_{TG}^0 as a function of V_{BG} is shown in Figure 5a. As the temperature decreases, a systematic positive shift in the threshold voltage is observed, which is attributed to enhanced localization and reduced thermal activation of carriers.[19,30,32] In addition, the transition of I_{TG}/I_{TG}^0 becomes sharper at lower temperatures, indicating a more abrupt onset of carrier accumulation. This behavior reflects a reduction in the number of band-tail states and a narrowing of the DOS distribution near the band edge.

To accurately extract C_q at different temperatures, the temperature dependences of C_{BG} and C_{TG} must be considered. Because both dielectric layers consist of HfO_2, we assume that their capacitances scale identically with the temperature. The scaling factor is determined from the depletion regime current I_{TG}^0, where C_q is negligible and the measured response is dominated by oxide capacitances. Figure 5b shows the ratio $I_{TG}^0(T)/I_{TG}^0(295\ K)$, which exhibits a monotonic decrease with temperature. The approximately 14% reduction inferred

https://doi.org/10.1021/acs.nanolett.6c04248
Nano Lett. XXXX, XXX, XXX−XXX

Downloaded from pubs.acs.org/naletd/article-pdf/doi/10.1021/acs.nanolett.6c04248/6921837/2/acs.nanolett.6c04248.pdf?guestAccessKey=e86e5cae-4f7e-4602-8685-84094555cb16 by PURDUE UNIV user on 18 November 2026

from the depletion current ratio is comparable in magnitude to previously reported reductions in HfO_2 permittivity of approximately 9%[33] and 12%[34] at cryogenic temperatures. These reports support the approximate magnitude of the temperature correction, while the common fractional scaling of C_{BG} and C_{TG} is adopted as a modeling approximation. This ratio is used to calibrate C_{BG} and C_{TG} at each temperature prior to the C_q extraction.

The extracted C_q as a function of V_{BG} at different temperatures is presented in Figure 5c. A pronounced reduction in C_q is observed in the negative bias region (−3 to −2 V) as the temperature decreases. No separate correction for thermal broadening is applied during extraction; its effects remain embedded in the measured response. The observed reduction is consistent with a reduced screening contribution from localized band-tail states at low temperature,[30,31] while reduced thermal broadening may also contribute. As a result, the measured C_q in this regime becomes closer to the ideal theoretical prediction that excludes the disorder-related effects. At high positive V_{BG}, C_q exhibits a relatively weak temperature dependence, consistent with the fact that the total DOS is largely temperature-independent. The remaining discrepancy between the measured C_q in this regime is attributed to residual states related to disorders of the channel and uncertainties in the oxide capacitance calibration.

These results demonstrate that eFPT enables direct tracking of temperature-dependent electronic-state evolution, revealing the crossover from disorder-dominated transport near the threshold to more intrinsic channel behavior at high carrier density. This capability further confirms the effectiveness of eFPT for probing C_q and provides insights into the role of disorder and localization in OS channels.

QUANTUM CAPACITANCE IN DIFFERENT THICKNESSES AND COMPOSITIONS

Finally, to systematically evaluate the tunability of C_q in OS channels, we investigate In-based FETs with varying channel thicknesses and compositions. Three different InO_x thicknesses and three different IGZO compositions were prepared. Their corresponding transfer characteristics are shown in Figure S4, exhibiting systematic threshold voltage shifts with the thickness and composition.[20,35] Notably, the 2.8-nm-thick InO_x device and all IGZO devices possess comparable channel thicknesses (~2.5−3 nm), enabling a meaningful comparison of the composition-dependent effects.

Figure 6a shows extracted C_q as a function of n_s, obtained from five devices under each condition. A clear thickness dependence is observed, with thicker InO_x channels exhibiting larger C_q over the measured n_s range. Devices with 3.8-nm-thick InO_x channels show incomplete turn-off and elevated leakage current at small device dimensions (Figure S5a). However, larger-area devices suppress leakage and recover the expected trend of increased C_q with thickness (Figure S5b,c). These results indicate that increasing the channel thickness enhances the accessible DOS, resulting in higher quantum capacitance.

In addition, postdeposition annealing of the 2.8-nm-thick InO_x channel at 300 °C leads to a steeper increase in C_q at low n_s, suggesting reduced disorder and a sharper band-edge DOS.[30,31] At high carrier density, however, the extracted C_q approaches values similar to those of the 250 °C annealed film. High-temperature annealing primarily modifies near-edge band-tail states rather than the total high-energy DOSs.

Figure 6b shows the composition dependence of IGZO channels with similar thicknesses. A systematic enhancement in C_q is observed with an increasing In fraction. This trend suggests that C_q in ultrathin OSs cannot be described solely by conventional effective mass-based DOS models. Instead, C_q is governed not only by the band effective mass but also by the band-tail states, disorder-induced DOS redistribution, and Fermi-level positioning. Consequently, In-rich channels exhibit larger C_q values than Ga/Zn-rich compositions.

Figure 6c shows extracted C_q at a fixed high carrier density ($n_s = 3.4 \times 10^{13}$ cm^{-2}, 295 K). The horizontal axis represents the In ALD cycle fraction, defined as the number of In deposition cycles divided by the total number of In, Ga, and Zn deposition cycles in the recipe. This parameter does not represent a measured atomic In fraction; however, it provides a clearly defined basis for a qualitative comparison of the film compositions and their associated C_q values. Distinct thickness- and composition-dependent trends are evident, demonstrating that the quantum capacitance can be systematically tuned through material design. These findings establish C_q as an engineerable parameter in OS FETs and highlight a practical pathway toward optimizing the CET, electrostatic control, and scaling performance in next-generation devices.

In this work, we demonstrated the direct experimental measurement of C_q in In-based OS FETs using eFPT. This approach overcomes the key limitations of conventional EOT-based estimations and enables the unambiguous extraction of channel C_q. The robustness of the measurement was verified under varying frequencies, AC voltage amplitudes, device areas, and bottom dielectric thicknesses, due to the implementation of lock-in detection, which offers clear advantages over conventional LCR-meter-based $C-V$ measurements.

The experimentally extracted and theory-based C_q results reveal three main contributions: first subband occupation, second subband occupation, and band nonparabolicity. Nevertheless, quantitative discrepancies between measured and calculated values remain because of additional electronic states, including band-tail states, trap states, and disorder effects originating from the structural disorder of the OS film. Temperature-dependent measurements additionally reveal suppression of localized tail-state contributions at low temperatures, while C_q in the fully accumulated regime remains comparatively unchanged. Higher In contents and thicker films produce larger C_q experimentally.

Beyond the n-type OS channels investigated here, this implementation could be adapted to other thin-body semiconductor systems. Because eFPT probes electronic screening, its operating principle is applicable to both electron- and hole-conducting channels. Potential platforms include 2D semiconductors and other thin-film transistor systems with accessible gates on the opposite sides of the channel. Reliable extraction requires sufficiently low gate leakage, controlled parasitic coupling, calibrated gate dielectric capacitances, and an electrostatic model appropriate to the channel geometry. Charge relaxation through the channel and contacts must also be evaluated at the measurement frequency.

METHODS

Atomic Layer Deposition (ALD) Growth of the Double-Gate In-Based OS FETs

To minimize parasitic capacitance arising from coupling between the Si substrate, metal pads, and channel, high-resistivity Si substrates (>10,000 Ω·cm) with 300 nm of SiO_2 were used. A 10 nm Al_2O_3

https://doi.org/10.1021/acs.nanolett.6c04248
Nano Lett. XXXX, XXX, XXX−XXX

Downloaded from pubs.acs.org/naletd/article-pdf/doi/10.1021/acs.nanolett.6c04248/6921837/2/acs.nanolett.6c04248.pdf?guestAccessKey=e86e5cae-4f7e-4602-8685-84094555cb16 by PURDUE UNIV user on 18 November 2026

adhesion layer was first deposited by plasma-enhanced atomic layer deposition (PEALD), using $Al(CH_3)_3$ (TMA) as the precursor.

A 35 nm Ni bottom-gate electrode was then deposited by electron-beam (e-beam) evaporation. HfO_2 bottom-gate dielectric layers with varying thicknesses were subsequently deposited at 200 °C by plasma-enhanced ALD (PEALD), using $[(CH_3)_2N]_4Hf$ (TDMAHf). InO_x films with different thicknesses and IGZO films with varying compositions were deposited at 225 °C by thermal ALD to form the channel layers, using $(CH_3)_3In$ (TMIn), $(C_2H_5)_2Zn$ (DEZ), $Ga_2(NMe_2)_6$, and H_2O.

Channel regions with various device dimensions were patterned using an AZ1518 photoresist and a Heidelberg MLA150 maskless aligner. Following lithographic definition of the source/drain (S/D) regions, a 35 nm Ni layer was deposited by e-beam evaporation as the contact metal. Channel isolation was achieved by dry etching using a Plasma-Therm Apex SLR ICP-RIE instrument.

A 12 nm HfO_2 top-gate dielectric layer was subsequently deposited at 150 °C by PEALD, followed by deposition of a 50 nm Ni top-gate electrode by e-beam evaporation. Finally, postmetallization annealing was carried out in a Jipelec rapid thermal annealing system at 250 or 300 °C for 1 min in an oxygen (O_2) ambient.

Double-Gate In-Based OS FET Device Characterization

Electrical transfer characteristics were measured by using a Keysight B1500 system. Dielectric capacitances were measured by using an Agilent E4980A LCR meter.

Electric-field penetration measurements were performed using an SR830 lock-in amplifier together with a Keithley 2450 sourcemeter. Temperature-dependent measurements (7−295 K) were conducted in a Lake Shore CRX-VF cryogenic probe station.

Quantum Capacitance Calculation

The theoretical quantum capacitance of the InO_x channel was modeled using an effective DOS comprising contributions from the first two subbands and a phenomenological correction for band nonparabolicity:

$$C_q^{th}(\mu) = e^2 \int_0^\infty dE\, DOS(E) \frac{-\partial f(E-\mu)}{\partial E} \quad (2)$$

where $DOS(E)$ is the density of states per unit area, $f(E)$ is the Fermi−Dirac distribution, and e is the elementary charge. Both E and the chemical potential μ are referenced to the modeled conduction band edge E_c, taken as the onset of the first subband.

The bias-dependent chemical potential was estimated from the measured capacitance using the approximate electrostatic relationship

$$\mu(V_{BG}) - \mu(V_{th}) = e \int_{V_{th}}^{V_{BG}} \frac{C_{BG}}{C_{BG} + C_{TG} + C_q(V')} dV' \quad (3)$$

where $C_q(V_{BG})$ is the experimentally extracted quantum capacitance and $\mu(V_{th}) = 0$ is assumed. All capacitances are expressed per unit area. V_{th} is extracted using linear extrapolation from the I_D-V_{BG} curve, and the value was −2.46 V.

Using this approximation, μ reaches approximately 0.2 eV at the highest measured positive back-gate bias. To describe this low-energy range, we adopted a simplified DOS model retaining the first two subbands. The approximately parabolic dispersion near each subband edge was represented by a steplike DOS, while band nonparabolicity was incorporated through a linear-energy-dependent correction:

$$DOS_{fsb}(E) = D_0\Theta(E) \quad (4)$$

$$DOS_{ssb}(E) = D_0\Theta(E - E_2) \quad (5)$$

$$DOS_{np}(E) = sE \quad (6)$$

Here Θ represents the Heaviside step function, $D_0 = m^*/\pi\hbar^2$, m^* is the effective electron mass, and $\hbar$ is the reduced Planck constant. The subscripts fsb, ssb, and np denote the first subband, second subband, and band nonparabolicity correction, respectively. The first subband begins at $E = E_c$, and E_2 denotes the second subband onset relative to E_c.

The nonparabolicity coefficient was set to $s = 7.9 \times 10^{13}$ eV^{-2} cm^{-2}. An effective mass of $m^* = 0.3m_0$, where m_0 is the free electron mass, was adopted based on the value reported for crystalline In_2O_3.[36,37] The corresponding subband capacitance scale and nonparabolicity slope are approximately $e^2D_0 = 20.04$ μF cm^{-2} and $e^2s = 12.64$ μF cm^{-2} eV^{-1}, respectively.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.6c04248.

Additional details for oxide capacitance for varying thickness, extracted quantum capacitance from different frequencies and AC voltages, quasi-static behavior verification, transfer characteristic InO_x, and IGZO FETs data (PDF)

■ AUTHOR INFORMATION

Corresponding Author

Peide D. Ye − *Elmore Family School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, United States;* orcid.org/0000-0001-8466-9745; Email: yep@purdue.edu

Authors

Kisoo Nam − *Elmore Family School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, United States*

Chang Niu − *Elmore Family School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, United States;* orcid.org/0000-0003-3175-7164

Aravindh Shankar − *Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907, United States;* orcid.org/0009-0006-5133-7641

Jian-Yu Lin − *Elmore Family School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, United States;* orcid.org/0000-0002-8800-8714

Sanjeev Khare − *Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907, United States*

Sumi Lee − *Elmore Family School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, United States*

Pramey Upadhyaya − *Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907, United States*

Complete contact information is available at: https://pubs.acs.org/10.1021/acs.nanolett.6c04248

Author Contributions

†K.N. and C.N. contributed equally to this work. P.D.Y. supervised the project. K.N. and C.N. fabricated the devices and performed the measurements. K.N., C.N., A.S., J.-Y.L., S.K., and S.L. analyzed the data. A.S. and S.K. conducted theory-based calculations under the supervision of P.U.. K.N., C.N., and P.D.Y. wrote the manuscript, and all the authors commented on it.

Downloaded from pubs.acs.org/nalefd/article-pdf/doi/10.1021/acs.nanolett.6c04248/6921837/acs.nanolett.6c04248.pdf?guestAccessKey=e86e5cae-4f7e-4602-8685-84094555cb16 by PURDUE UNIV user on 18 November 2026

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

P.D.Y. and P.U. were supported by the internal Blue Sky Project at Purdue University. P.D.Y. was also supported in part by the U.S. National Science Foundation under Award 2425498 with industry partners as specified in the Future of Semiconductors (FuSe2) program, Semiconductor Research Corporation Global Research Program and Samsung Electronics, Inc. (Grant IO250514-12841-01).

■ REFERENCES

(1) Dennard, R. H.; Gaensslen, F. H.; Yu, H.-N.; Rideout, V. L.; Bassous, E.; LeBlanc, A. R. Design of Ion-Implanted MOSFETs with Very Small Physical Dimensions. *IEEE J. Solid-State Circuits* **1974**, *9* (5), 256−268.

(2) Mack, C. A. Fifty Years of Moore's Law. *IEEE Trans. Semicond. Manuf.* **2011**, *24* (2), 202−207.

(3) Chau, R. Advanced Metal Gate/High-k Dielectric Stacks for High-Performance CMOS Transistors. *AVS 5th International Microelectronics Interfaces Conference*; AVS, 2004; pp 3−5.

(4) Ko, J.-S.; Shearer, A. B.; Lee, S.; Neilson, K.; Jaikissoon, M.; Kim, K.; Bent, S. F.; Pop, E.; Saraswat, K. C. Achieving 1-nm-Scale Equivalent Oxide Thickness Top-Gate Dielectric on Monolayer Transition Metal Dichalcogenide Transistors with CMOS-Friendly Approaches. *IEEE Trans. Electron Devices* **2025**, *72* (3), 1514−1520.

(5) Park, H.; Kirtania, S. G.; Sarkar, E.; Chakraborty, D.; Zhang, C.; Lee, H.-J.; Shin, J.; Yu, S.; Khan, A.; Kim, H.; Im, C.; Hong, M. J.; Ha, D.; Datta, S. Demonstration of Tungsten-Doped Indium Oxide MOSFETs with 3 Angstrom EOT, Improved Stability and High On-Current. *IEEE Symposium on VLSI Technology and Circuits*; IEEE, 2025.

(6) Park, H.; Kirtania, S. G.; Sarkar, E.; Chakraborty, D.; Zhang, C.; Lee, H. J.; Shin, J.; Yu, S.; Khan, A.; Kim, H.; Im, C.; Hong, M. J.; Ha, D.; Datta, S. Extreme EOT Scaling in Tungsten-Doped In_2O_3 MOSFETs for Enhanced Stability and Drive Current. *IEEE Trans. Electron Devices* **2025**, *72* (12), 7136−7144.

(7) Vasileska, D.; Schroder, D. K.; Ferry, D. K. Scaled Silicon MOSFET's: Degradation of the Total Gate Capacitance. *IEEE Trans. Electron Devices* **1997**, *44* (4), 584−587.

(8) Bennett, R. K. A.; Pop, E. How Do Quantum Effects Influence the Capacitance and Carrier Density of Monolayer MoS2 Transistors? *Nano Lett.* **2023**, *23*, 1666−1672.

(9) Jin, D.; Kim, D.; Kim, T.; del Alamo, J. A. Quantum Capacitance in Scaled Down III−V FETs. *2009 IEEE International Electron Devices Meeting (IEDM)*; IEEE, 2009; pp 1−4.

(10) Ganeriwala, M. D.; Yadav, C.; Mohapatra, N. R.; Khandelwal, S.; Hu, C.; Chauhan, Y. S. Modeling of Charge and Quantum Capacitance in Low Effective Mass III-V FinFETs. *IEEE J. Electron Dev Soc.* **2016**, *4* (6), 396−401.

(11) Charnas, A.; Zhang, Z.; Lin, Z.; Zheng, D.; Zhang, J.; Si, M.; Ye, P. D. Review-Extremely Thin Amorphous Indium Oxide Transistors. *Adv. Mater.* **2024**, *36*, No. 2404014.

(12) Datta, S.; Dutta, S.; Grisafe, B.; Smith, J.; Srinivasa, S.; Ye, H. Back-End-of-Line Compatible Transistors for Monolithic 3-D Integration. *IEEE Micro.* **2019**, *39* (6), 8−15.

(13) Si, M.; Lin, Z.; Chen, Z.; Ye, P. D. High-Performance Atomic-Layer-Deposited Indium Oxide 3-D Transistors and Integrated Circuits for Monolithic 3-D Integration. *IEEE Trans. Electron Devices* **2021**, *68* (12), 6605−6609.

(14) Niu, C.; Tan, P.; Lin, J.-Y.; Long, L.; Lin, Z.; Zhang, Y.; Wang, H.; Wilk, G. D.; Ye, P. D. First Demonstration of BEOL Wafer-Scale All-ALD Channel CFETs Using IGZO and Te for Monolithic 3D Integration. *IEEE International Electron Devices Meeting (IEDM)*; IEEE, 2024.

(15) Lin, J.-Y.; Zhang, Z.; Lin, Z.; Niu, C.; Zhang, Y.; Zhang, Y.; Kim, T.; Jang, H.; Sung, C.; Hong, M.; Lee, S. M.; Lee, T.; Cho, M. H.; Ha, D.; Jeong, C.; Wang, H.; Alam, M. A.; Ye, P. D. First Demonstration of Top-Gate Enhancement-Mode ALD In2O3 FETs with High Thermal Budget of 600 °C for DRAM Applications. *IEEE Electron Device Lett.* **2024**, *45* (10), 1851−1854.

(16) Charnas, A.; Lin, Z.; Zhang, Z.; Ye, P. D. Atomically Thin In_2O_3 Field-Effect Transistors with 10^{17} Current On/Off Ratio. *Appl. Phys. Lett.* **2021**, *119*, No. 263503.

(17) Lin, Z.; Niu, C.; Jang, H.; Kim, T.; Zhang, Y.; Wang, H.; Jeong, C.; Ye, P. D. Enhancement of In_2O_3 Field-Effect Mobility up to 152 $cm^2\ V^{-1}\ s^{-1}$ Using HZO-Based Higher-*k* Linear Dielectric. *IEEE Symposium on VLSI Technology and Circuits*; IEEE, 2024.

(18) Lin, Z.; Si, M.; Askarpour, V.; Niu, C.; Charnas, A.; Shang, Z.; Zhang, Y.; Hu, Y.; Zhang, Z.; Liao, P.-Y.; Cho, K.; Wang, H.; Lundstrom, M.; Maassen, J.; Ye, P. D. Nanometer-Thick Oxide Semiconductor Transistor with Ultra-High Drain Current. *ACS Nano* **2022**, *16*, 21536−21545.

(19) Niu, C.; Lin, Z.; Zhang, Z.; Tan, P.; Si, M.; Shang, Z.; Wang, H.; Ye, P. D. Record-Low Metal to Semiconductor Contact Resistance in Atomic-Layer-Deposited In_2O_3 TFTs Reaching the Quantum Limit. *IEEE International Electron Devices Meeting (IEDM)*; IEEE, 2023.

(20) Lee, S.; Niu, C.; Zhang, Y.; Wang, H.; Ye, P. D. Positive to Negative Schottky Barrier Transition in Metal/Oxide Semiconductor Contacts by Tuning Indium Concentration in IGZO. *IEEE Symposium on VLSI Technology and Circuits*; IEEE, 2024.

(21) Dröscher, S.; Roulleau, P.; Molitor, F.; Studerus, P.; Stampfer, C.; Ensslin, K.; Ihn, T. Quantum Capacitance and Density of States of Graphene. *Appl. Phys. Lett.* **2010**, *96*, No. 152104.

(22) Ma, N.; Jena, D. Carrier Statistics and Quantum Capacitance Effects on Mobility Extraction in Two-Dimensional Crystal Semiconductor Field-Effect Transistors. *2D Mater.* **2015**, *2*, No. 015003.

(23) Kraus, P. A.; Ahmed, K. Z.; Williamson, J. S., Jr. Elimination of Chuck-Related Parasitics in MOSFET Gate Capacitance Measurements. *IEEE Trans. Electron Devices* **2004**, *51* (8), 1350−1352.

(24) Tao, J.; Zhao, C. Z.; Zhao, C.; Taechakumput, P.; Werner, M.; Taylor, S.; Chalker, P. R. Extrinsic and Intrinsic Frequency Dispersion of High-k Materials in Capacitance-Voltage Measurements. *Materials* **2012**, *5*, 1005−1032.

(25) Eisenstein, J. P.; Pfeiffer, L. N.; West, K. W. Negative Compressibility of Interacting Two-Dimensional Electron and Quasiparticle Gases. *Phys. Rev. Lett.* **1992**, *68* (5), 674−677.

(26) Eisenstein, J. P.; Pfeiffer, L. N.; West, K. W. Compressibility of the Two-Dimensional Electron Gas: Measurements of the Zero-Field Exchange Energy and Fractional Quantum Hall Gap. *Phys. Rev. B* **1994**, *50* (3), 1760−1778.

(27) Allison, G.; Galaktionov, E. A.; Savchenko, A. K.; Safonov, S. S.; Fogler, M. M.; Simmons, M. Y.; Ritchie, D. A. Thermodynamic Density of States of Two-Dimensional GaAs Systems near the Apparent Metal-Insulator Transition. *Phys. Rev. Lett.* **2006**, *96*, No. 216407.

(28) Li, L.; Richter, C.; Paetel, S.; Kopp, T.; Mannhart, J.; Ashoori, R. C. Very Large Capacitance Enhancement in a Two-Dimensional Electron System. *Science* **2011**, *332*, 825−828.

(29) Wu, Y.; Chen, X.; Wu, Z.; Xu, S.; Han, T.; Lin, J.; Skinner, B.; Cai, Y.; He, Y.; Cheng, C.; Wang, N. Negative Compressibility in Graphene-Terminated Black Phosphorus Heterostructures. *Phys. Rev. B* **2016**, *93*, No. 035455.

(30) Niu, C.; Charnas, A.; Lin, J.-Y.; Long, L.; Lin, Z.; Zhang, Z.; Ye, P. D. Breakdown of Ohm's Law by Disorders in Low-Dimensional Transistors. *Nano Lett.* **2026**, *26*, 4839−4846.

(31) Niu, C.; Nam, K.; Shankar, A.; Lin, J.-Y.; Khare, S.; Lee, S.; Upadhyaya, P.; Ye, P. D. Size-Dependent Band-Tail Localization in Oxide Semiconductors Revealed by Direct Density-of-States Mapping. *arXiv* **2026**.

(32) Wang, J.; Bi, J.; Xu, G.; Liu, M. Characteristics Analysis of IGZO TFT and Logic Unit in the Temperature Range of 8−475 K. *Electronics* **2024**, *13*, 1427.

Downloaded from pubs.acs.org/naletd/article-pdf/doi/10.1021/acs.nanolett.6c04248/6921837/2/acs.nanolett.6c04248.pdf?guestAccessKey=e86e5cae-4f7e-4602-8685-84094555cb16 by PURDUE UNIV user on 18 November 2026

https://doi.org/10.1021/acs.nanolett.6c04248
Nano Lett. XXXX, XXX, XXX−XXX

(33) Paghi, A.; Battisti, S.; Tortorella, S.; De Simoni, G.; Giazotto, F. Cryogenic Behavior of High-Permittivity Gate Dielectrics: The Impact of Atomic Layer Deposition Temperature and the Lithographic Patterning Method. *J. Appl. Phys.* **2025**, *137*, No. 044103.
(34) Biercuk, M. J.; Monsma, D. J.; Marcus, C. M.; Becker, J. S.; Gordon, R. G. Low-Temperature Atomic-Layer-Deposition Lift-Off Method for Microelectronic and Nanoelectronic Applications. *Appl. Phys. Lett.* **2003**, *83*, 2405−2407.
(35) Lee, S.; Niu, C.; Shih, C.-A.; Lin, J.-Y.; Zhang, Z.; Zhang, Y.; Long, L.; Wang, H.; Alam, M. A.; Ye, P. D. Comprehensive Study of Low-Frequency Noise Origins in Scaled Atomic-Layer-Deposited IGZO TFTs. *IEEE Trans. Electron Devices* **2025**, *72* (6), 2993−2999.
(36) Niu, C.; Lin, Z.; Askarpour, V.; Zhang, Z.; Tan, P.; Si, M.; Shang, Z.; Zhang, Y.; Wang, H.; Lundstrom, M. S.; Maassen, J.; Ye, P. D. Surface Accumulation Induced Negative Schottky Barrier and Ultralow Contact Resistance in Atomic-Layer-Deposited In_2O_3 Thin-Film Transistors. *IEEE Trans. Electron Devices* **2024**, *71* (5), 3403−3410.
(37) Preissler, N.; Bierwagen, O.; Ramu, A. T.; Speck, J. S. Electrical Transport, Electrothermal Transport, and Effective Electron Mass in Single-Crystalline In_2O_3 Films. *Phys. Rev. B* **2013**, *88*, No. 085305.

Downloaded from pubs.acs.org/naletd/article-pdf/doi/10.1021/acs.nanolett.6c04248/6921837 2/acs.nanolett.6c04248.pdf?guestAccessKey=e86e5cae-4f7e-4602-8685-84094555cb16 by PURDUE UNIV user on 18 November 2026

https://doi.org/10.1021/acs.nanolett.6c04248
Nano Lett. XXXX, XXX, XXX−XXX